WHAT IS CLAIMED IS:

1. A system for testing a circuit design using a test generator, comprising:

a random number generator, operating responsive to a seed, for generating a random number sequence;

an event probability generator, operating responsive to profile settings, for generating a probability profile,

wherein said test generator, responsive to said random number sequence and said probability profile, is operable to generate a test case that includes settings indicative of said seed and said profile settings, said test case for exercising a model of said circuit design; and

an extraction and regeneration engine operable to extract said seed and said profile settings from a test structure related to said test case in order to generate a reconstituted test case for further testing of said circuit design.

2. The system as recited in claim 1, wherein said seed and said profile settings are extracted from said test structure in order to provide said extracted seed and profile settings to a modified test generator, wherein said modified test generator is modified to avoid illegal test behavior with respect to said test case.

3. The system as recited in claim 1, wherein said test structure comprises said test case.

4. The system as recited in claim 1, wherein said test structure comprises a test file generated upon executing said test case on said circuit design.

5. The system as recited in claim 1, wherein said circuit design model comprises a simulated processor model that simulates the behavior of said circuit design with software.

6. The system as recited in claim 1, wherein said circuit design model comprises a processor core including at least one processor for operating at least one thread.

7. The system as recited in claim 1, wherein said circuit design model comprises a register-transfer level (RTL) model of an integrated circuit.

8. The system as recited in claim 1, wherein said circuit design model comprises an architectural simulation model of an integrated circuit.

9. The system as recited in claim 1, wherein said profile settings relate to controlling the probability of an event selected from the list of events consisting of loading, storing, arithmetic operations, and floating-point operations.

10. The system as recited in claim 1, wherein said extraction and regeneration engine is operable to extract command line settings from said test structure.

11. The system as recited in claim 1, wherein said test structure comprises a test file that contains at least one illegal test behavior.

12. The system as recited in claim 1, wherein said extraction and regeneration engine is implemented in a software language selected from the group consisting of a C, C++, and Perl.

13. A method of testing a circuit design using a test generator, comprising:

detecting an illegal test behavior in a test file produced upon exercising a test case generated by the test generator on a model of the circuit design;

extracting profile settings from a test structure relating to said test case;

extracting a random number seed from said test structure;

reconstructing input data supplied to said test generator from said profile settings and said random number seed extracted from said test structure; and

supplying said reconstructed input data to a modified test generator, wherein said modified test generator is modified to avoid said illegal test behavior.

14. The method as recited in claim 13, wherein the operations of extracting profile settings, extracting a random number seed, and reconstructing input data are performed automatically.

15. The method as recited in claim 13, further comprising employing a comparator to modify said test generator to produce said modified test generator.

16. The method as recited in claim 13, further comprising debugging said test generator.

17. The method as recited in claim 13, further comprising extracting command line settings from said test structure.

18. The method as recited in claim 17, wherein the operation of reconstructing input data comprises reconstructing input data supplied to said test generator from said profile settings, said random number seed, and said command line settings.

19. A computer system operable to simulate a platform for testing a circuit design, the computer system comprising:

test generator means for generating a test case using a random number seed and an event probability profile, said test case for executing on a model associated with said circuit design;

means for extracting and regenerating said random number seed and said event probability profile from a test structure relating to said test case; and

means for automatically retesting said circuit design model using a reconstituted test case based on said extracted random number seed and event probabilities profile.

20. The computer system as recited in claim 19, wherein said circuit design model comprises a simulated processor model that simulates the behavior of said circuit design with software.

21. The computer system as recited in claim 19, wherein said circuit design model comprises a processor core including at least one processor for operating at least one thread.

22. The computer system as recited in claim 19, wherein said circuit design model comprises a register-transfer level (RTL) model of an integrated circuit.

23. The computer system as recited in claim 19, wherein said circuit design model comprises an architectural simulation model of an integrated circuit.

24. The computer system as recited in claim 19, wherein said profile settings relate to controlling the probability of an event selected from the list of events consisting of loading, storing, arithmetic operations, and floating-point operations.

25. The computer system as recited in claim 19, wherein said reconstituted test case is further based on command line settings extracted from said test structure.

26. The computer system as recited in claim 19, wherein said test structure comprises a test file containing at least one illegal test behavior, said test file being generated upon executing said test case on said circuit design model.

27. A system for testing a circuit design using a test generator, comprising:

means for detecting an illegal test behavior in a test file produced upon exercising a test case generated by the test generator on a model of the circuit design;

means for extracting profile settings from a test structure relating to said test case;

means for extracting a random number seed from said test structure;

means for reconstructing input data supplied to said test generator from said profile settings and said random number seed; and

means for supplying said reconstructed input data to a modified test generator, wherein said modified test generator is modified to avoid said illegal test behavior.

28. The system as recited in claim 27, wherein said means for extracting profile settings, means for extracting a random number seed, and means for reconstructing input data operate automatically.

29. The system as recited in claim 27, further comprising comparator means to modify said test generator to produce said modified test generator.

30. The system as recited in claim 27, further comprising means for debugging said test generator.

31. The system as recited in claim 27, further comprising means for extracting command line settings from said test structure.

32. The system as recited in claim 31, wherein said means for reconstructing input data comprises means for reconstructing input data supplied to said test generator from said profile settings, said random number seed, and said command line settings.

33. A method for debugging a test generator, comprising:

verifying a test case generated by said test generator;

automatically extracting profile settings from said test case;

automatically extracting a random number seed from said test case;

automatically reconstituting test input parameters from said extracted profile settings and said random number seed; and

supplying said reconstituted input parameters to said test generator for debugging.

34. The method as recited in claim 33, further comprising extracting command line settings from said test case.

35. The method as recited in claim 34, wherein the operation of automatically reconstituting input parameters from said extracted profile further comprises automatically reconstituting test input parameters from said extracted profile settings, said random number seed, and said command line settings.

36. The method as recited in claim 34, wherein the operation of supplying said reconstituted input parameters to said test generator for debugging further comprises supplying said reconstituted input parameters to said test generator for debugging by a comparator.

37. A system for debugging a test generator, comprising:

means for verifying a test case generated by said test generator;

means for automatically extracting profile settings from said test case;

means for automatically extracting a random number seed from said test case;

means for automatically reconstituting test input parameters from said extracted profile settings and said random number seed; and

means for supplying said reconstituted input parameters to said test generator for debugging.

38. The system as recited in claim 37, further comprising means for extracting command line settings from said test case.

39. The system as recited in claim 38, wherein said means for automatically reconstituting input parameters from said extracted profile further comprises means for automatically reconstituting test input parameters from said extracted profile settings, said random number seed, and said command line settings.

40. The system as recited in claim 37, wherein said means for supplying said reconstituted input parameters to said test generator for debugging further comprises means for supplying said reconstituted input parameters to said test generator for debugging by a comparator.

41. A computer-readable medium operable with a computer platform for testing a circuit design using a test generator, the medium having stored thereon:

instructions for detecting an illegal test behavior in a test file produced upon exercising a test case generated by the test generator on a model of the circuit design;

instructions for extracting profile settings from a test structure relating to said test case;

instructions for extracting a random number seed from said test structure;

instructions for reconstructing input data supplied to said test generator from said profile settings and said random number seed extracted from said test structure; and

instructions for supplying said reconstructed input data to a modified test generator, wherein said modified test generator is modified to avoid said illegal test behavior.

42. A computer-readable medium operable with a computer platform for debugging a test generator, the medium having stored thereon:

instructions for verifying a test case generated by said test generator;

instructions for automatically extracting profile settings from said test case;

instructions for automatically extracting a random number seed from said test case;

instructions for automatically reconstituting test input parameters from said extracted profile settings and said random number seed; and

instructions for supplying said reconstituted input parameters to said test generator for debugging.